

LSI Logic Corporation Legal Department – IP 1621 Barber Lane, MS D-106 Milpitas, CA 95035

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From: Connie del Castillo
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Conie del Cartillo

Connie del Castillo

Cophone

Telephone No. (408) 433-7191

Fax No.

(408) 433-7460

	Urgent	☐ For your review	1	Reply ASAP		Please comment
Application Number Filing date: First named inventor Attorney docket number Transmitted herewith  Status Reque	r: <u>Cam</u> ) aber: <u>03-197</u> for filing via	nber 3, 2003 Lu et al. 78 / 81641				
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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Cam Lu et. al.

Serial No.:

10/728,036

Filed:

December 03, 2003

For:

Method of Generating an Efficeint Stuck-At Fault and Transition Delay

Fault Truncated Scan Test Pattern for an Integrated Circuit Design 888

Group Art Unit:

2825

Examiner:

Atty Docket:

81641 / 03-1978

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## STATUS REQUEST

Commissioner for Patents P. O. Box 1450

Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

LSI Logic Corporation 1621 Barber Lane, MS D-106 Milipitas, CA 95035 [+1] 408-433-7191

Date: 6 DEC OY

Respectfully submitted,

25TR End

Timothy Croll, Ph: [+1] 408-433-7191

Reg. No. 36,771